

S03P1450

SPECIFICATION

AUDIO AMPLIFIER

5 TECHNICAL FIELD

This invention relates to an audio amplifier.

BACKGROUND ART

10 In an audio amplifier, if a power amplifier of a final stage is configured with a so-called D-class amplifier, a whole is able to be digitized, and is able to be configured as a digital audio amplifier.

Fig. 3 shows one example of such digital audio amplifier. . Namely, a digital audio signal S11 is supplied to an over-sampling circuit 12 from an input terminal 11, a sampling frequency thereof is over-sampled to be a digital signal S12 of 8 times, this digital signal
15 S12 is supplied to a $\Delta\Sigma$ modulation circuit 14 through a variable attenuator circuit 13 for volume control, and is re-quantized to be bit-reduced digital signal S14. Further, this digital signal S14 is supplied to a PWM modulation circuit 15, and converted to a PWM signal S15, then this PWM signal S15 is supplied to a power amplifier 16 operating in D-class.

20 This power amplifier 16 is configured with a switching circuit for power amplifying by switching a power source voltage in accordance with the PWM signal S15, and a low pass filter for outputting a D/A converted and power amplified analog audio signal by smoothing the switching output. Further, by the power amplifier 16, the power amplified audio signal is supplied to a speaker 30 through an output terminal 17.

25 Further, in a system controller (not illustrated), a volume control signal SVOL is formed, and this signal SVOL is supplied to the variable attenuator circuit 13 as a control

signal. Accordingly, when a switch for the volume control is operated, an attenuation level of the variable attenuator circuit 13 is changed, and a volume of a reproduced sound outputted from the speaker 30 is changed.

Further, in this case, the $\Delta\Sigma$ modulation circuit 14 includes a feedback loop for a quantizing error, so that even if a content of the digital signal S12 supplied from the variable attenuator circuit 13 to the $\Delta\Sigma$ modulation circuit 14 is zero, a digital signal S14 having something value is accordingly outputted from the $\Delta\Sigma$ modulation circuit 14, and the digital signal S14 is accordingly outputted from the speaker 30 as a noise sound having a specified frequency.

Consequently, in a dither signal forming circuit 18, a dither signal SDI of a minute level is formed, this dither signal SDI is supplied to the $\Delta\Sigma$ modulation circuit 14, and is superimposed on the digital signal S12 upon re-quantization. Accordingly, even in a case where the content of the digital signal S12 outputted from the variable attenuator circuit 13 is zero, an actual content of the $\Delta\Sigma$ modulation circuit 15 does not become zero, so that it is suppressed to output the noise sound.

Further, in a case when the digital signal S11 to be supplied to the input terminal 11 is switched or disconnected by the switching of the source devices supplying the digital signal S11, the synchronization of the digital signal S11 is temporary disturbed, and this disturbance of synchronization is accordingly outputted from the speaker 30 as the noise sound.

For the sake, the digital signal S11 supplied to the input terminal 11 is supplied to an asynchronous detection circuit 19, and a disturbance of synchronization of the digital signal S11 is detected. Further, this detection signal SDET is supplied to the circuits 12 to 14 as a muting signal, and when the synchronization of the digital signal S11 is disturbed, the contents of the signals S12 and S14 are set to be zero, and as the result, the reproduced sound outputted from the speaker 30 is muted.

The above is one example of an audio amplifier where the power amplifier 17 in the final stage is configured with a D-class amplifier (See Japanese Laid-open Patent Application OP2002-158543, for example).

By the way, in case of the audio amplifier as shown in Fig. 3, when a muting is performed by the detection signal SDET of the asynchronous detection circuit 19, not only the digital signal S12 is muted, but also the dither signal SDI is simultaneously muted in the $\Delta\Sigma$ modulation circuit 14. Accordingly, the dither signal SDI is abruptly cutoff upon muting, and a noise signal is generated by this abrupt cutoff, so that this is outputted from the speaker 30 as a noise sound.

Further, though the dither signal SDI has a minute level, the presence/absence of the dither signal SDI is able to be recognized as a difference in a noise level. Therefore, when the muting is set to be on, the noise level changes because the dither signal SDI is muted, but in a case where the content of the input digital signal S11 is zero (or a minute level), the change in the noise level is recognized, and this causes uncomfortable feeling.

This invention is to solve the above problems.

DISCLOSURE OF THE INVENTION

According to the present invention, an audio amplifier is configured to include, for example, a sampling rate converter circuit for performing a sampling rate conversion of a first digital audio signal with a first clock synchronized thereto and a second clock having a predetermined frequency into a second digital audio signal synchronized with the second clock, a $\Delta\Sigma$ modulation circuit for re-quantizing the second digital audio signal into a third digital audio signal having reduced number of bits, a PWM modulation circuit for converting the third digital audio signal into a PWM signal, a D-class power amplifier to be supplied the PWM signal outputted from the PWM modulation circuit, a dither signal forming circuit for superimposing a dither signal on the third digital audio signal by

supplying the dither signal to the $\Delta\Sigma$ modulation circuit, and a muting signal forming circuit, wherein an input side of the sampling rate converter circuit is stopped by a muting signal upon muting.

Accordingly, the dither signal is continuously supplied to the $\Delta\Sigma$ modulation circuit even during muting, and the digital audio signal including the dither signal is supplied to the D-class power amplifier after converting into the PWM signal.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a system chart designating one mode of the present invention.

Fig. 2 is a chart for describing the present invention.

Fig. 3 is a system chart for describing the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Fig. 1 shows one example of a digital audio amplifier 10 according to the present invention, and a digital audio signal S11 is supplied to an over-sampling circuit 12 through an input terminal 11. Further, the digital signal S11 from the input terminal 11 is supplied to a PLL 21, a clock SPLL synchronized with the digital signal S11 and having a frequency of n times of its sampling frequency is formed, and thus generated clock SPLL is supplied to the over-sampling circuit 12 as a clock for over-sampling. In this case, the magnification n of the over-sampling is set to be a value as shown in Fig. 2 corresponding to the sampling frequency of the digital signal S11.

Thus, in the over-sampling circuit 12, the digital signal S11 supplied thereto is over-sampled to a digital signal S12 synchronized with the signal S11, and having a frequency of n times the sampling frequency.

And, this digital signal S12 is supplied to the sampling rate converter circuit 23 as a conversion input. Further, the clock SPLL from the PLL 21 is supplied to the sampling

rate converter circuit 23 as a clock for conversion input side.

Further, the clock forming circuit 22 is configured with a crystal oscillation circuit, and a dividing circuit, and a clock SGEN having a frequency of 49.152 MHz ($= 48 \text{ kHz} \times 1024$) with a stable frequency and a phase is derived from this clock forming circuit 22.

5 Then, this clock SGEN is supplied to the sampling rate converter circuit 23 as a clock of conversion output side. Thus, in the sampling rate converter circuit 23, the digital signal S12 supplied thereto is converted into a digital signal S23 having a sampling frequency which is a frequency of 384 kHz ($= 48 \text{ kHz} \times 8$), for example, with a stable frequency and a phase.

10 Then, the sampling rate converted digital signal S23 is supplied to the variable attenuator circuit 13 for the volume control, the level thereof is controlled by the control signal SVOL from the system controller (not illustrated), the level controlled digital signal S12 is supplied to the $\Delta\Sigma$ modulation circuit 14, and is re-quantized into a bit-reduced digital signal S14. By the way, in the dither signal forming circuit 18, the dither signal
15 SDI of a minute level is formed at this time, and this dither signal SDI is superimposed on the digital signal S23 to be supplied to the $\Delta\Sigma$ modulation circuit 14.

Then, the digital signal S14 re-quantized by the $\Delta\Sigma$ modulation circuit 14 is supplied to the PWM modulation circuit 15, and is converted into a PWM signal S15. This PWM signal S15 is then supplied to the power amplifier 16 operating in D class, and
20 power amplified, and after that, thus amplified output is supplied to the speaker 30 through the output terminal 17.

At this time, the clock SGEN from the forming circuit 22 is supplied to the circuits 13 to 15, and 18 as their clocks. Accordingly, the output side of the sampling rate converter circuit 23 and the circuits 13 to 15, and 18 are to be operated in synchronism
25 with the clock SGEN.

Further, the digital signal S11 supplied to the input terminal 11 is supplied to the

asynchronous detection circuit 19, also the clock having a frequency equal to the sampling frequency of the input digital signal S11 and synchronized thereto is derived from the PLL 21, this clock is supplied to the asynchronous detection circuit 19, and a disturbance of the synchronization of the digital signal S11 supplied to the input terminal 11 is detected.

5 Then, the detection signal SDET is supplied to the over-sampling circuit 12, an input side of the sampling rate converter circuit 23, and the variable attenuator circuit 13 as a muting signal, and when a synchronization of the digital signal S11 is disturbed, the content of the signal S12 is set to be zero, and also the operation of the input side in the sampling rate converter circuit 23 is stopped.

10 According to the above-mentioned configuration, the digital audio signal S11 supplied to the input terminal 11, in spite of its sampling frequency, the sampling frequency is converted its sampling rate into the digital signal having a sampling frequency of 384 kHz by the sampling rate converter circuit 23, and after that, it is power amplified after converted into the PWM signal S15, then supplied to the speaker 30.

15 Further, as a result of switching or disconnecting the digital signal S11 to be supplied to the input terminal 11 by the switching of the source devices supplying the digital signal S11, the synchronization of the digital signal S11 is temporary disturbed, and this disturbance of synchronization is detected by the asynchronous detection circuit 19, and by the detection signal SDET, the over-sampling circuit 12 and the input side of the sampling rate converter circuit 23 are stopped. Accordingly, the digital signal S12 is to
20 be shut out during an interval of the detection signal SDET.

However, even the operation of the input side in the sampling rate converter circuit 23 during the interval of the detection signal SDET is stopped, the digital signal S23 is continuously outputted from the sampling rate converter circuit 23, because the output side
25 thereof is supplied with the clock SGEN, and the operation is continuous.

However in this case, as the operation of the input side in the sampling rate

converter circuit 23 is stopped and the detection signal SDET is also supplied to the variable attenuator circuit 13, the content of the digital signal S23 outputted from the variable attenuator circuit 13 is zero.

Then, such digital signal S23 is supplied to the $\Delta\Sigma$ modulation circuit 14, and the
5 detection signal SDET is not supplied to the $\Delta\Sigma$ modulation circuit 14, during the interval of the detection signal SDET, the digital signal S14 the content of which is zero is outputted from the $\Delta\Sigma$ modulation circuit 14, and this digital signal S14 is supplied to the PWM modulation circuit 15. Accordingly, during the interval of the detection signal SDET, a muting is activated to the input audio signal S11. That is, the interval of the
10 detection signal SDET is the muting interval.

As described above, the digital audio amplifier shown in FIG. 1, the muting is performed, however, even during the muting interval, the dither signal SDI is supplied to the $\Delta\Sigma$ modulation circuit 14, and accordingly, even if the content of the digital signal S23 supplied thereto is zero, it never happens to output from the $\Delta\Sigma$ modulation circuit 14 the
15 signal components which become a noise sound of a particular frequency.

Further, even during the muting interval, the dither signal SDI is supplied to the $\Delta\Sigma$ modulation circuit 14, the noise levels become equal between when the muting is off and when the muting is on. Accordingly, in a case when the content of the input digital signal S11 is zero (or, a minute level), if a muting is activated, there is no fear of being
20 recognized the change in the noise level and uncomfortable feeling.

Further, when changing from a state where the muting is off to a state where the muting is on, and when changing from a state where the muting is on to a state where the muting is off, the dither signal SDI is always continuing, so that there is no fear of generating noise signals, and also there is no fear of outputting a noise sound from the
25 speaker 30.

(List of abbreviations used in this specification)

D/A : Digital to Analog

PLL : Phase Locked Loop

PWM : Pulse Width Modulation

5 Industrial Applicability

According to the present invention, even if a muting is on when the content of the input digital audio signal is zero, or a minute level, there is no fear of uncomfortable feeling due to the recognition of the change in the noise level. Further, when the muting is made on from the muting off state, or when the muting is released from the muting on state, there is no fear of generating noise signals, and also there is no fear of outputting a noise sound from the speaker.